AMENDMENTS TO THE CLAIMS[1]

1. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

forming a semiconductor element in a semiconductor active region, the semiconductor active region being in an electrically floating state, and calculating ~~the~~ a generation rate of electron hole pairs caused by impact ionization in said semiconductor element;

calculating a volume integral of said generation rate of electron hole pairs ~~at least~~ in an area where the impact ionization is caused;

evaluating time-dependent variations of electrical characteristics of said semiconductor element on the basis of said volume integral; and

manufacturing a semiconductor device based on ~~the basis of evaluation~~ results of the evaluating step.

2. (Currently Amended) The method of claim 1, wherein[[:]] calculating the generation rate of electron hole pairs ~~is performed by~~ comprises calculating the generation rate of electron hole pairs in an insulated gate field effect transistor formed in said semiconductor active region on an insulating layer of a substrate; and

evaluating time-dependent variations of electrical characteristics of said semiconductor element ~~is performed by~~ comprises evaluating time-dependent variations of electrical characteristics of said insulated gate field effect transistor.

3. (Currently Amended) The method of claim 1, wherein[[:]] calculating said generation rate of electron hole pairs ~~is performed by~~ comprises calculating the generation

[1] This listing of claims will replace all prior versions, and listings, of claims in the application.

rate of electron hole pairs in an insulated gate field effect transistor formed in said semiconductor active region on an insulating layer on a substrate or in said semiconductor active region on a sapphire substrate; and

evaluating time-dependent variations of electrical characteristics of said semiconductor element ~~is performed by~~ comprises evaluating time-dependent variations of electrical characteristics of said insulated gate field effect transistor.

4. (Cancelled)

5. (Currently Amended) The method of claim 1, wherein calculating said generation rate of electron hole pairs ~~is performed by~~ comprises calculating the generation rate of electron hole pairs in an insulated gate field effect transistor formed in a semiconductor active region without any well electrode or body electrode; and

evaluating time-dependent variations of electrical characteristics of said semiconductor element ~~is performed by~~ comprises evaluating time-dependent variations of electrical characteristics of said insulated gate field effect transistor.

6. (Currently Amended) The method of claim 1, wherein evaluating time-dependent variations of electrical characteristics of said semiconductor element ~~is performed by~~ comprises evaluating time-dependent variations of a threshold voltage of an insulated gate field effect transistor on the basis of variations ΔV_{th} of a threshold voltage derived using the following equation

$$\Delta V_{th} = A \left(\frac{I_{subQ}}{Id} \right)^{\alpha} Id^{\beta}$$

~~where~~ wherein I_{subQ} denotes a pseudo current of a semiconductor active region, Id denotes a drain current, and A, α, and β denote model parameters.

7. (Currently Amended) The method of claim 1, wherein evaluating time-dependent variations of electrical characteristics of said semiconductor element ~~is performed by~~ comprises evaluating time-dependent variations of a driving current of an insulated gate field effect transistor.

8. (Currently Amended) The method of claim 1, wherein evaluating time-dependent variations of electrical characteristics of said semiconductor element ~~is performed by~~ comprises creating data concerning the relationship between stresses and variations of a threshold voltage in a certain time period under the stresses, and by evaluating time-dependent variations of a threshold voltage of an insulated gate field effect transistor on the basis of said data.

9. (Currently Amended) The method of claim 8, wherein evaluating time-dependent variations of said electrical characteristics of said semiconductor element ~~is performed by~~ comprises evaluating time-dependent variations of a threshold voltage of said insulated gate field effect transistor on the basis of empirically created or actually collected data representing at least the relationship between a predetermined current and variations of the threshold voltage.

10. (Currently Amended) The method of claim 1, wherein evaluating time-dependent variations of said semiconductor element ~~is performed by~~ comprises creating data concerning stresses at operating temperatures and variations of a threshold voltage in a certain time

period under the stresses, and by evaluating on the basis of said data time-dependent variations of the threshold voltage of an insulated gate field effect transistor in operation.

11. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

forming a semiconductor element in a semiconductor active region, the semiconductor active region being in an electrically floating state, and calculating the generation rate of electron hole pairs caused by impact ionization in said semiconductor element;

calculating a volume integral of said generation rate of electron hole pairs ~~at least~~ in an area where the impact ionization is caused;

calculating a time integral of physical quantities including the volume integral;

evaluating time-dependent variations of electrical characteristics of said semiconductor element on the basis of said time integral; and

manufacturing a semiconductor device based on ~~the basis of evaluation~~ results of the evaluating step.

12. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

forming a first insulated gate field effect transistor having a body contact electrode in a first semiconductor active region on an insulated film layer ~~at least~~ on a substrate, measuring at least a body current of said first semiconductor active region and creating data concerning at least said body current;

forming a second insulated gate field effect transistor without a body contact electrode in a second semiconductor active region, the second semiconductor active region being in an

electrically floating state, on said insulated film layer, and calculating the generation rate of electron hole pairs caused by impact ionization in said second insulated gate field effect transistor;

calculating a volume integral of said generation rate of electron hole pairs ~~at least~~ in a region where impact ionization is caused;

calculating time-dependent variations of electrical characteristics of said second insulated gate field effect transistor on the basis of said volume integral and ~~at least~~ the body current in said data; and

manufacturing a semiconductor device on the basis of said calculated time-dependent variations of said electrical characteristics.

13. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

performing initial designing of a semiconductor element to be formed in a semiconductor active region, the semiconductor active region being in an electrically floating state;

calculating the generation rate of electron hole pairs caused by impact ionization in said semiconductor element;

calculating a volume integral of said generation rate of electron hole pairs ~~at least~~ in a region where said impact ionization is caused;

evaluating time-dependent variations of electrical characteristics of said semiconductor element on the basis of said volume integral; and

redesigning said semiconductor element based on ~~the basis of evaluation~~ results of the evaluating step.

14. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

forming a semiconductor element in a semiconductor active region, the semiconductor active region being in an electrically floating state, and calculating the generation rate of electron hole pairs caused by impact ionization in said semiconductor element;

calculating a volume integral of said generation rate of electron hole pairs ~~at least~~ in a region where said impact ionization is caused;

calculating a physical model quantity after application of stresses to said semiconductor element, on the basis of said volume integral;

evaluating time-dependent variations of electrical characteristics after application of stress to said semiconductor element, on the basis of said calculated physical model quantities; and

manufacturing a semiconductor device based on ~~the basis of evaluation~~ results of the evaluating step.

15. (Currently Amended) The method of claim 14, wherein calculating the physical model quantity of said semiconductor element ~~is performed by~~ comprises calculating at least a density of an interface level on an interface of a gate insulating film of an insulated gate field effect transistor, a charge density measured in a gate insulating film or channel carrier mobility.

16. (Currently Amended) The method of claim 14, wherein forming said semiconductor element in said semiconductor active region is performed in accordance with the initial designing, the method further comprising:

evaluating time-dependent variations of electrical characteristics of said semiconductor element; and

redesigning said semiconductor element based on ~~the basis of evaluation~~ results of the evaluating step.

17. (Withdrawn) A semiconductor device comprising:

a substrate provided with an insulated layer at least on a surface thereof:

a first semiconductor active region on said insulated layer of said substrate;

a first insulated gate field effect transistor formed in said first semiconductor active region, provided with a body contact electrode and used for detecting a body current;

a second semiconductor active region on said insulated layer of said substrate; and

a second insulated gate field effect transistor formed in said second semiconductor active region and having no body contact electrode.

18. (Withdrawn) The semiconductor device of claim 17, wherein said substrate and said first and second semiconductor regions constitute a silicon-on-insulator structure or a silicon-on-sapphire structure.

19. (Withdrawn) An electrical characteristic evaluating system comprising:

a data inputting unit inputting physical model quantity data of a semiconductor element;

a data processing unit calculating on the basis of said input data the generation rate of electron hole pairs caused by impact ionization in said semiconductor element, calculating a volume integral of the generation rate of electrode hole pairs at least in a region where the

impact ionization is caused, and calculating time-dependent variations of said semiconductor element at least on the basis of said volume integral; and

a data outputting unit for outputting the calculated time-dependent variations of electrical characteristics.

20. (Withdrawn) The electrical characteristic evaluating system of claim 19, wherein said data processing unit uses software for the calculations of the generation rate of electron hole pairs, volume integral and time-dependent variations of electrical characteristics.

21. (Withdrawn) An evaluation business performing method comprising:

forming a semiconductor element in a semiconductor activation region;

calculating the generation rate of electron hole pairs caused by impact ionization in said semiconductor element;

calculating a volume integral of said generation rate of electron hole pairs at least in a region where said impact ionization is caused;

evaluating time-dependent variations of electrical characteristics of said semiconductor element on the basis of said volume integral; and

informing clients of evaluation results as business.

22. (Withdrawn) The method of claim 21, wherein said evaluation results are delivered to clients who are going to use semiconductor devices or who are actually using semiconductor devices.